In The Claims:

1. - 5. (Cancelled)

6. (Original) A integrated circuit device, comprising:

a semiconductor substrate having an upper surface, electrical components being formed in the semiconductor substrate;

a plurality of metal layers on top of the upper surface of the substrate, conductive paths defined in the metal layers being connected to the electrical components; and

a plurality of bonding pads disposed on top of the metal layers and connected thereto such that the electrical components are connected to selected bonding pads through the conductive paths, each bonding pad further comprising:

a bonding area located above a region where each of the metal layers overlaps; and

an elongated probing area located above a subset of the plurality of metal layers for receiving a probing pin of a probing card, the elongated probing area being electrically connected to the bonding area.

7. (Original) The integrated circuit device of claim 6, wherein the elongated probing area has a long dimension and a short dimension and the bonding area is connected to the short dimension of the elongated probing area.

8. (Original) The integrated circuit device of claim 7, wherein the long dimension of the elongated probing area is at least 75 microns long.

9. (Original) The integrated circuit device of claim 6, wherein the bonding area is substantially a square.

10. (Original) The integrated circuit device of claim 6, wherein the elongated probing area is substantially a rectangle.

11. (Presently Amended) A integrated circuit device, comprising:

a semiconductor substrate having an upper surface, the substrate further comprising an inner area and an outer area, the inner area hosting a plurality of electrical components

connected through a plurality of conductive paths disposed on the upper surface of the substrate; and

a plurality of bonding pads disposed on the conductive paths and connected thereto, each bonding pad further comprising:

a bonding area connected to at least of one of the conductive paths and located on top of the outer area of the substrate for receiving a bonding wire; and

an elongated probing area connected to the bonding area and located on top of the inner area of the substrate for receiving a probing pin of a probing card;

wherein the bonding area is located above a region where all the conductive paths overlap and the probing area is located above a region where less than all the conductive paths overlap.

12. (Original) The integrated circuit device of claim 11, wherein the bonding area is located over and connected to a stack of metal layers and at least one of the metal layers are connected to at least one of the conductive paths.

13. (Original) The integrated circuit device of claim 12, wherein the stack of metal layers are on top of a portion of the upper surface of the substrate that does not host the electrical components.

14. (Original) The integrated circuit device of claim 11, wherein the elongated probing area comprises one metal layer and at least one of the electrical components is directly below the probing area.

15. (Original) The integrated circuit device of claim 11, wherein the bonding area is substantially a square and the elongated probing area is substantially a rectangle.

16. (Original) The integrated circuit device of claim 11, wherein the elongated probing area has a long dimension and a short dimension and the bonding area is connected to the short dimension of the elongated probing area.

17. (Original) The integrated circuit device of claim 11, wherein the long dimension of the elongated probing area is at least 75 microns long.